What is claimed is:

1. In a computer system, a method for transferring portions of a memory block comprising the steps of:

(a) configuring a first data mover with a first start address corresponding to a first portion of a source memory block;

(b) configuring a second data mover with a second start address corresponding to a second portion of the source memory block sized differently from the first portion;

(c) transferring, by the first data mover, the first portion of the source memory block; and

(d) transferring, by the second data mover, the second portion of the source memory block.

2. The method of claim 1 further comprising configuring the first data mover with a first chunk end address corresponding to the first portion of the source memory block.

3. The method of claim 2 further comprising generating the first chunk end address.

4. The method of claim 1 further comprising configuring the first data mover with a first write address corresponding to a first portion of a first target memory block.

5. The method of claim 2 wherein the transferring of the first portion of the source memory block further comprises stopping when the first start address is substantially equivalent to the first chunk end address.

6. The method of claim 2 wherein the transferring of the first portion of the source memory block further comprises stopping when the first start address is substantially equivalent to a predefined end address.

7. The method of claim 1 further comprising configuring the second data mover with a second chunk end address.

8. The method of claim 7 further comprising generating the second chunk end address.

9. The method of claim 7 further comprising configuring the second data mover with a second write address corresponding to a second portion of a second target memory block.

10. The method of claim 7 wherein the transferring of the second portion of the source memory block further comprises stopping when the second start address is substantially equivalent to the second chunk end address.

11. The method of claim 7 wherein the transferring of the second portion of the source memory block further comprises stopping when the second start address is substantially equivalent to a predefined end address.

12. The method of claim 1 further comprising configuring the first data mover as a master data mover and the second data mover as a slave data mover.

13. The method of claim 12 further comprising communicating, by the master data mover, the first start addresses to the slave data mover.

14. The method of claim 4 further comprising transferring the first portion of the source memory block to the first write address corresponding to the first portion of the first target memory block.

15. The method of claim 10 further comprising transferring the second portion of the source memory block to the second write address corresponding to the second portion of the second target memory block.

16. The method of claim 1 further comprising substantially simultaneously transferring the first portion and the second portion of the source memory block.

17. In a computer system, a method for transferring portions of a memory block comprising the steps of:

(a) designating a master data mover;

(b) designating a slave data mover in communication with the master data mover;

(c) transmitting a start address to the master data mover, the start address identifying a first memory portion of a source memory block;

(d) transmitting the start address to the slave data mover to enable the slave data mover to determine a next address, the next address identifying a second memory portion of the source memory block sized differently from the first memory portion;

(e) transmitting a first write address identifying a first memory portion of a target memory block to the master data mover and a second write address identifying a second memory portion sized differently than the first memory portion of the target memory block to the slave data mover;

(f) copying the first memory portion of the source memory block to the first write address identifying the first memory portion of the target memory block; and

(g) transferring the second memory portion of the source memory block to the second write address identifying the second memory portion of the target memory block.

18. The method of claim 17 further comprising the steps of:

(h) verifying that the master data mover is available;

(i) transmitting a first end address associated with the first memory portion of the source memory block to the master data mover and a second end address associated with the second memory portion to the slave data mover; and

(j) synchronizing the master data mover with the slave data mover.

19. The method of claim 17 further comprising the steps of:

(h) transmitting a first offset address to the master data mover and a second offset address to the master data mover;

(i) obtaining, by the master data mover, a first next address by using the first offset address and the start address;

(j) obtaining, by the slave data mover, a second next address by using the second offset address and the start address;

(k) stopping the transmitting of the first memory portion of the source memory block after the first next address is substantially equivalent to the first end address; and

(l) stopping the transmitting of the second memory portion of the source memory block after the second next address is substantially equivalent to the second end address.

20. A system to transfer portions of a memory block comprising:

(a) a first data mover;

(b) a second data mover in communication with the first data mover over a DM communications bus;

(c) a first memory component having a first portion and a second portion sized differently from the first portion and in communication with the first data mover and the second data mover over a first DM-memory bus; and

a second memory component in communication with the first data mover and the second data mover over a second DM-memory bus,

wherein the first data mover transfers the first memory portion to the second memory component over the first DM-memory bus at a first data transfer rate, and

wherein the second data mover transfers the second memory portion to the second memory component over the second DM-memory bus at a second data transfer rate.

21. The system of claim 20 wherein the first DM-memory bus is a Peripheral Component Interconnect (PCI) bus and the second DM-memory bus is an Accelerated Graphics Port (AGP) bus.

22. The system of claim 20 wherein the first data mover transfers the first memory portion at a substantially simultaneous time as the second data mover transfers the second memory portion.

23. The system of claim 20 wherein the first data mover is a first Direct Memory Access (DMA) engine and the second data mover is a second DMA engine.